Arm Cortex M3 Instruction Set Summary

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Table 3.1. Cortex-M3 instructions; Mnemonic Operands Brief description Flags See; ADC, ADCS {Rd,} Rn, Op2. Add with Carry: N,Z,C,V: ADD, ADC, SUB, SBC, and RSB: ADD, ADDS {Rd,} Rn, Op2. Add: N,Z,C,V: ADD, ADC, SUB, SBC, and RSB: ADD, ADDW {Rd,} Rn, #imm12. Add: N,Z,C,V: ADD, ADC, SUB, SBC, and RSB: ADR: Rd, label. Load PC-relative Address-ADR: AND, ANDS {Rd,} Rn, Op2. Logical AND: N,Z,C

Cortex-M3 Devices Generic User Guide | Instruction set ...
ARM DUI 0552A: Non-Confidential: ID121610 PDF version: Home > The Cortex-M3 Instruction Set > Miscellaneous instructions > SEV ...

Cortex-M3 Devices Generic User Guide: 3.10.9. SEV
3.5.1 Syntax.....64 3.5.2 Operation.....64

Cortex-M3/M4F Instruction Set Technical User's Manual (Rev. A)
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Cortex-M3 Technical Reference Manual
State-of-the-art Arm® Cortex®-M3 MCU series Small footprint. The small footprint of the core allows it to be used either as a single core in small devices or as an additional embedded companion core when specific hardware isolation or task partitioning is required. Thanks to the advancements in silicon manufacturing technologies, the lithography process moved from 180 to 90nm and lower, and the core silicon real-estate now reaches 0.03mm² in 90nm lithography.

Arm Cortex-M3 - Microcontrollers - STMicroelectronics
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Documentation – Arm Developer
ARM Instruction Set ARM7TDMI-S Data Sheet 4-5 ARM DDI 0084D 4.2 The Condition Field In ARM state, all instructions are conditionally executed according to the state of the CPSR condition codes and the instruction's condition field. This field (bits 31:28) determines the circumstances under which an instruction is to be executed. If the state

4 ARM Instruction Set - Université Laval
ISO/IEC C code cannot directly access some Cortex-M3 instructions. This section describes intrinsic functions that can

generate these instructions, provided by the CMSIS and that might be provided by a C compiler. If a C compiler does not support an appropriate intrinsic function, you might have to use inline assembler to access some instructions.

Cortex-M3 Devices Generic User Guide - Arm Developer

Set Architecture (continued) The Cortex-M3 supports only the Thumb-2 (and traditional Thumb) instruction set. Instead of using ARM instructions for some operations, as in traditional ARM processors, it uses the Thumb-2 instruction set for all operations. As a result, the Cortex-M3 processor is not backward

ARM - 32-bit Microcontroller - Shrishail Bhat

The ARM Cortex-M is a group of 32-bit RISC ARM processor cores licensed by Arm Holdings.These cores are optimized for low-cost and energy-efficient microcontrollers, which have been embedded in tens of billions of consumer devices. The cores consist of the Cortex-M0, Cortex-M0+, Cortex-M1, Cortex-M3, Cortex-M4, Cortex-M7, Cortex-M23, Cortex-M33, Cortex-M35P, Cortex-M55.

ARM Cortex-M - Wikipedia

ARM State Instruction Set Features o 3-address data processing instructions o Conditional execution of each instruction o Shift and ALU operations in single instruction o Load-Store and Load-Store multiple instructions o Single cycle execution of all instructions o Instruction set extension through coprocessor instructions N. Mathivanan 4.

Arm instruction set - SlideShare

On the other extreme we can say that Cortex-M4 is basically a cortex-M3 profile with the integration of a DSP unit in it. The instruction set architecture used in cortex-M4 is Thumb-2 which is a mixture of 32 bit ARM instruction set architecture and 16 bit Thumb instruction set architecture.

ARM Cortex-M4 Architecture - Microcontrollers Programming

This video presents the basics of the Cortex-M architecture from the programmer's point of view, including the registers and the memory map.

01: ARM Cortex-M Instruction Set Architecture - YouTube

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Technical Reference Manual - ARM architecture

The Cortex-M3 processor implements a version of the Thumb®instruction set based on Thumb-2 technology, ensuring high code density and reduced program memory requirements. The Cortex-M3 instruction set provides the exceptional performance expected of a modern 32-bit architecture, with the high code density of 8-bit and 16-bit microcontrollers.

~~Cortex-M3 Devices - ARM architecture~~

, ARM is the most widely used instruction set architecture (ISA) and the ISA produced in the largest quantity. Currently, the widely used Cortex cores, older "classic" cores, and specialized SecurCore cores variants are available for each of these to include or exclude optional capabilities.